METHOD AND MOTHERBOARD FOR AUTOMATICALLY DETERMINING MEMORY TYPE

CROSS REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90107335, filed on March 28, 2001.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates in general to a technique for determining the memory type, and more particularly, the invention relates to an automatic determining mechanism of a motherboard that support various types of memories.

Description of the Related Art

[0002] Dynamic random access memory (DRAM) plays an important role in the field of personal computers. As techniques develop and cost is reduced, the types and capacity of the dynamic random access memory continuously progress. The most popular dynamic random access memory on the market includes the synchronous dynamic random access memory (SDRAM). Inevitably, the SDRAM is replaced as technique progresses. Currently, the double data rate dynamic random access memory (DDR DRAM) is the representative product of the next generation. However, as the technique is not fully developed yet, it is still too expensive. Therefore, in the transition time of two generations, a motherboard that accommodates both the SDRAM and the DDR DRAM is produced in personal computer industry. The operation voltage such as

I/O supply voltage for the DDR DRAM is 2.5V, while the operation voltage for the SDRAM is 3.3V. The mixed DRAM motherboard provides the jumper to let the user to configure the type of DRAM. However, this confuses the user and easily causes man-made mistake in operation, consequently damaging the equipment. Therefore, a mechanism to automatically determine the type of DRAM is necessary.

[0003] Currently, most computer systems provide several power saving modes like suspend to RAM (STR) mode or suspend to disk (STD) mode. No matter the computer system is reset or rebooted after soft off, mechanical off, or STD mode, the mixed DRAM motherboard must have a mechanism to redetect the type of DRAM. When the computer system enters the STR mode, the motherboard has to maintain a configured operation voltage to prevent memory from data loss or from damage.

SUMMARY OF THE INVENTION

[0004] The invention provides a method and a motherboard for automatically determining the type of memory. By applying the characteristic of having different operation voltage for different DRAM modules, a software program is used to test the DRAM modules and generate a control signal to automatically adjust the DRAM control voltage, so as to achieve the automation determination of the type of DRAM. Therefore, the DRAM module is protected and operated normally.

[0005] The present invention provides a method of automatically determining a type of a memory applied in a computer system, comprises the steps of outputting a preset voltage to the memory; performing an operation on the memory; determining a type of the memory; outputting a control signal; outputting a voltage adjustment signal according to the control signal and the system power state signal; and outputting a configured

operation voltage to the memory according to the voltage adjustment signal.

[0006] The present invention further provides a motherboard to automatically determine a type of a memory, comprises a hardware device, at least one memory module slot, a voltage control circuit, and a recognition apparatus. The hardware device generates a control signal. The memory module slot accommodates a memory. The voltage control circuit couples to the memory module slot to provide a configured operation voltage to the memory module slot. The recognition apparatus couples to the system power state signal, the control signal and the voltage control circuit. In this way, the voltage control circuit firstly outputs a preset voltage to the memory and then the hardware device outputs the control signal after performing an operation to determine a type of the memory, and then the recognition apparatus outputs a voltage adjustment signal after receiving the control signal and the system power state signal, so that the voltage control circuit outputs the configured operation voltage to the memory.

[0007] Both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 shows an embodiment of a computer system according to the invention;

[0009] Figure 2 shows the internal circuit of a recognition apparatus; and

[0010] Figure 3 is a flow chart showing the method provided by the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0011] Figure 1 shows an embodiment of a computer system according to the invention. In Figure 1, a motherboard 110 comprises a system power state signal (SUSC) 210, a voltage control circuit 140, a processor (central processing unit, CPU) 120, and a recognition apparatus 100. The processor 120 executes a software program to generate a control signal 200 to the recognition apparatus 100. Obviously, the processor executing the software program is only one embodiment of the invention. Any hardware device working like a processor executing the same software program and generating the control signal 200 can be utilized in the present invention. The present invention does not limit the device generating the control signal 200.

[0012] After decoding the control signal 200 and the system power state signal (SUSC) 210, the recognition apparatus 100 of the motherboard 110 outputs a voltage adjustment signal 220 to the voltage control circuit 140. The function of the software program is to determine the used type of the DRAM by accessing the memory in the memory module slot 130. The recognition apparatus 100 then determines what the current system state is, generates the proper voltage adjustment signal 220 and sends the voltage adjustment signal to the voltage control circuit 140. The system power state can be obtained from the system power state signal (SUSC) 210. If the system power state signal (SUSC) is a low logic state, the system is in a STD, a soft off mode, or mechanical off mode. The motherboard 110 then only provides a low configured operation voltage (such as 2.5V I/O supply voltage). When the system power state signal (SUSC) is a high logic state, the memory inserted in the memory module slot 130 requires a configured operation voltage. The motherboard must provide the SDRAM with a configured operation voltage of 3.3V, or provide the DDR DRAM with a configured operation

voltage of 2.5V according to the detected type of DRAM.

[0013] Figure 2 shows the internal circuit of a recognition apparatus 100 according to the invention. Referring to both Figures 1 and 2, the recognition apparatus 100 comprises a D-flip-flop such as an RS D-flip-flop 230. The RS D-flip-flop 230 receives a control signal 200 and a system power state signal (SUSC) 210 to generate a voltage adjustment signal 220 to the voltage control circuit 140 of the motherboard 110. The inverter has the input terminal coupled to the control signal 200 and an output terminal coupled to a D (data) terminal of an RS D-flip-flop 230. The control signal 200 is further coupled to a CLK (clock) terminal of the RS D-flip-flop 230. When the system power state signal (SUSC) 210 is the low logic state, since the system power state signal (SUSC) 210 is coupled to an CL (clear) terminal of the RS D-flip-flop 230, the output terminal #Q (that is, the voltage adjustment signal 220) is configured as a high logic state. The operation indicates that the system state is STD mode, soft off mode, or mechanical off mode. The voltage control circuit 140 only has to output a configured operation voltage of 2.5V to the memory in the memory module slot 130. When the system power state signal (SUSC) is a high logic state, the memory in the memory module slot 130 requires a configured operation voltage to provide the SDRAM or the DDR DRAM to normal active. If the control signal 200 is converted from the low logic state to the high logic state, the CLK terminal of the RS D-flip-flop 230 is triggered to send the delayed control signal 200 to the RS D-flip-flop 230. As a result, the voltage adjustment signal 220 coupled to the output terminal #Q is configured as a low logic state. The operation indicates that the type of DRAM in use is SDRAM and causes the voltage control circuit to output the configured operation voltage of 3.3V to the memory. In addition to the above description, the output terminal #Q of the RS D-flip-flop 230 is remains at the

previous logic state, so that the voltage control circuit keeps providing the same configured operation voltage. To correctly operate in the STR mode, STD mode, soft off mode, or mechanical off mode the recognition apparatus may uses a standby power source. The PR (preset) terminal of the RS D-flip-flop 230 is coupled to a specific voltage source to avoid affecting operation.

[0014] Figure 3 is a flow chart of a method for automatically determining the type of memory provided by the invention. When the computer system is power on (or the computer is rebooted from the STD, soft off, or mechanical off mode), the voltage control circuit firstly outputs 2.5V to the memory module in step 300. The computer system executes a software program to perform an accessing operation on the memory, and to determine whether the current memory module is functioning normally in step 310. If the type of DRAM in use is DDR DRAM, the control signal sent remains unchanged in step 320, and the voltage adjustment signal sent to the voltage control circuit is also unchanged in step 330. The voltage control circuit does not change the configured operation voltage of 2.5V after receiving the voltage adjustment signal in step 340. In the power on procedure, the voltage control circuit keeps outputting the configured operation voltage (2.5V) in step 350. In contrast, if the currently used type of memory is SDRAM, the control signal sent to the recognition apparatus is changed in step 322. The voltage adjustment signal sent from the recognition apparatus to the voltage control circuit is changed in step 332. In step 342, the voltage control circuit outputs a configured operation voltage of 3.3V. During the power on procedure, the voltage control circuit keeps outputting the configured operation voltage (3.3V) in step 350. When the computer system enters the STD mode, soft off mode, or mechanical off mode in step 360, the system power state signal SUSC enters the low logic state in step 370. A recognition

apparatus is provided to receive the system power state signal (SUSC) to determine whether the system is in the STD mode, soft off mode or mechanical mode. If the system is in these modes, the recognition apparatus ignores the result of the control signal and directly drives the voltage control circuit to provide the memory module with 2.5V in step 380. In the STR mode, an operation is performed with a previous voltage adjustment signal without changing to prevent memory from data loss or from damage in step 390. In addition, if the system is reset in step 400, the process goes back to step 310, and the computer system executes the software program to determine the type of the used memory module.

[0015] Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.